AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning at page 3, line 20, with the following rewritten paragraph:

Another approach as shown in Figure 5 4 is a delayed driving scheme which reduces the variation of the drain node voltage. The input synchronization is realized by using two traditional latches as implemented using switches 504, 506, 508, and 510 in front of the delayed driving block. As shown in Figure 6, the crossing points are lower than the middle point (VH+VL)/2 for PMOS output switches, 514 and 516; while the crossing points are higher than the middle point (VH+VL)/2 for NMOS output switches, 302 and 304 of Figures 3 and 4.